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APPLICATION FOR LETTERS PATENT

**Reducing Coupled Noise in Pseudo-Differential
Signaling Systems**

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TECHNICAL FIELD

The present invention relates to the transmission of data over transmission lines that are subject to capacitively and/or inductively coupled noise. More specifically, the present invention reduces the effect of such induced or coupled noise in systems using(pseudo-differential transmission lines).

BACKGROUND

Fig. 1 shows an electronic system that transmits data or other signals using pseudo-differential signaling. The system includes a first integrated circuit 10 that transmits the signals, and a second integrated circuit 12 that receives the signals. The signals comprise voltages that are conducted between the two integrated circuits by a plurality of signal lines 14. The signal lines are typically metallic traces on a printed circuit board.

In addition to the signals themselves, a reference voltage is transmitted from first integrated circuit 10 to second integrated circuit 12, over a reference line 16. The signal voltages represent values in terms of relationships between the signal voltages and the reference voltage. In a binary system, for example, a high voltage—one which is higher than the reference voltage—might represent a binary “1”. A low voltage—one that is less than the reference voltage—might represent a binary “0”.

Fig. 2 illustrates how the values of signal lines are determined within the receiving integrated circuit 12. A signal comparator 20, often in the form of a comparator, is associated with each signal voltage V_{SIG} . Each signal line is routed to a first input of the associated signal comparator 20. The reference voltage V_{REF} is routed in common to the second input of each signal comparator 20. The signal

1 comparator produces a high logic level within integrated circuit 12 if the signal
2 voltage is higher than the reference voltage. The signal comparator produces a
3 low logic level within integrated circuit 12 if the signal voltage is not higher than
4 the reference voltage.

5 This type of signaling technique reduces or cancels the effect of any
6 electrical noise that is induced in signal lines 14 between the two integrated
7 circuits. The technique works on the assumption that any noise induced in a signal
8 line will be similarly induced in the common reference line. This assumption, in
9 turn, relies on the further assumption that the signal lines are subject to the same
10 noise inducing influences as the reference line.

11 These assumptions are generally correct, at least to a degree. In high-speed
12 data transfer circuits, however, it is often desired to utilize very small differentials
13 {between "high" and "low" signal voltages. The use of such small voltage
14 differentials accentuates the effect of any differences in induced noise between the
15 signal lines and the reference line.

16 In sensitive circuits such as these, even small differences in induced noise
17 can become significant. One reason such differences arise is that the reference
18 line is routed to many more components than an individual signal line.
19 Specifically, a signal line is routed (within the receiving integrated circuit) to only
20 a single signal comparator. The reference line, on the other hand, is routed to all
21 of the signal comparators. Each connection to signal comparator introduces a new
22 source of noise coupling. Furthermore, additional routing lengths are usually
23 required to reach the signal comparators, which also adds coupling capacitance.

24 Fig. 3 shows a simplified model of a reference line 30 and a signal line 32.
25 The lines are driven by devices having equal output impedances, and the

1 transmission lines are carefully designed to have the same distributed line
2 impedances. The transmission line and driver impedances are represented as R_C in
3 Fig. 3.

4 At the receiving integrated circuit, the reference line and signal line are
5 connected to a package pin. This pin introduces a parasitic inductance L_I . Within
6 the integrated circuit, both of the lines are capacitively coupled to the substrate
7 (V_{SS}) of the integrated circuit. This coupling is mainly through the capacitances of
8 the input pad, existing electrostatic discharge (ESD) circuitry, and the inputs of the
9 signal comparators. Since the reference line drives a multitude of signal
10 comparators and has a longer routing path, its coupling capacitance C_{REF} is
11 significantly larger than the capacitance C_{IN} of the signal line. Moreover,
12 depending on the length and the resistivity of the reference routing wire, the
13 additional capacitance of the reference line may behave as a distributed RC line.

14 The capacitive coupling C_{REF} and C_{IN} result in noise injection from the
15 integrated circuit's power supply rails to the signal and reference lines. If C_{REF}
16 and C_{IN} were equal, the noise injection would be common mode and would not
17 affect the interpretation of the signal. But because C_{REF} is so much greater than
18 C_{IN} in (a pseudo-differential interface), the noise injection on the reference line is
19 fundamentally larger than that on the signal line. This results in a reduction of
20 common mode noise rejection by the signal comparators, especially at high
21 frequencies.

22 The technique described below reduces the effect of noise injection in
23 (pseudo-differential interfaces) such as shown in Figs. 1-3.

SUMMARY

In the circuits described below, the reference voltage is buffered in the receiving circuit prior to its distribution to the multiple signal comparators. In one embodiment, the buffered voltage is the sum of the reference voltage and its noise. In another embodiment, the buffered voltage represents only the noise.

The buffered voltage is used in each embodiment to account for the differences between impedances seen by the signal voltages and the relatively greater impedances seen by the reference voltage.

In one embodiment, the buffering is accomplished with an active buffer such as a unity gain operational amplifier, having a bandwidth that is significantly greater than the resonant input frequency of the reference and signal inputs.

Alternatively, both the signal voltages and the reference voltages are buffered using MOSFET source-followers. To reduce differential noise injection, the source-follower associated with the reference input is larger than the source-follower of the signal inputs by specific ratio. This ratio is equal to the ratio of the capacitance seen by the output of the source-follower associated with the reference line to the capacitance seen by the output of the source-follower associated with the signal line.

In another embodiment, the buffered voltage represents only the noise of the signal lines, and is subtracted from the signal voltages to remove the noise.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 illustrates a prior art pseudo-differential signaling system.

Fig. 2 illustrates receiving circuitry of a prior art pseudo-differential signaling system.

1 Fig. 3 illustrates electrical characteristics of signal and reference lines in a
2 prior art pseudo-differential signaling system.

3 Fig. 4 illustrates a pseudo-differential signaling system in which the
4 invention can be embodied.

5 Fig. 5 illustrates electrical characteristics of a receiving circuit in a pseudo-
6 differential signaling system.

7 Figs. 6 and 7 illustrate electrical characteristics of receiving circuits in
8 alternative embodiments of pseudo-differential signaling systems.

9
10 **DETAILED DESCRIPTION**

11 Fig. 4 shows a system 100 including a first integrated circuit 102 that
12 transmits pseudo-differential data signals in conjunction with a reference signal,
13 and a second integrated circuit 104 that receives the data and reference signals.
14 Specifically, the signals include a plurality of pseudo-differential data signal
15 voltages, referred to herein simply as signal voltages, and a single, common
16 reference voltage. These signals are conducted on corresponding pseudo-
17 differential signal lines 106 and a reference line 108.

18 The pseudo-differential data signals represent values in terms of
19 relationships between the signal voltages and the common reference voltage. In
20 the described embodiment, for example, a signal voltage that is higher than the
21 reference voltage represents a binary "1". A data signal voltage that is lower than
22 the reference voltage represents a binary "0".

23 Fig. 5 shows receiver circuitry, within receiving integrated circuit 104,
24 corresponding to the reference signal and one of the signal lines. Parasitic
25 inductance L_I is introduced on each signal line by the corresponding package pins

1 on the integrated circuit—the external pins to which the lines are routed from the
2 transmitting integrated circuit.

3 Each signal line is routed within integrated circuit 104 to a signal receiver
4 or comparator 110. Integrated circuit 104 has a plurality of such signal
5 comparators, corresponding respectively to each of the received pseudo-
6 differential signals.

7 With regard to the data signal lines, coupling capacitance is represented as
8 C_S . Noise is injected into each data signal line from the integrated circuit's
9 substrate V_{SS} through coupling capacitance C_S . C_S is a result of capacitances of
10 the input pad corresponding to the signal line, existing ESD circuitry, and the
11 input of the data signal comparator 110.

12 The reference voltage or signal is routed within the integrated circuit to a
13 reference receiver 112, before the reference voltage has been distributed to the
14 various signal comparators. In this embodiment, the reference receiver is an active
15 buffer. More specifically, reference receiver 112 is a unity gain amplifier—
16 preferably an operational amplifier—that receives the common reference voltage
17 and in response produces a buffered common reference voltage or signal V_{BUF} ,
18 also referred to herein as a buffered signal or voltage. The buffered voltage is
19 distributed to each of data signal comparators 110. Thus, each data signal
20 comparator compares or otherwise evaluates the buffered reference voltage and
21 the corresponding pseudo-differential signal voltage to determine the value
22 represented by the signal voltage.

23 In the described embodiment, each signal comparator comprises a
24 transistor-based comparator that compares two input voltages and produces a
25

1 binary voltage output that is dependent on which of the two input voltages is
2 greater. Optionally, the voltage output might be produced as a differential signal.

3 With regard to the reference line, coupling capacitance includes C_{R1} and
4 C_{R2} . C_{R1} represents coupling capacitance of the *unbuffered*, undistributed,
5 common reference signal, and is a result of capacitances of the input pad
6 corresponding to the reference line, ESD circuitry, and the input of active buffer
7 112. Noise is injected into the unbuffered reference line from the integrated
8 circuit's substrate V_{SS} through coupling capacitance C_{R1} . Active buffer 112 is
9 designed to have an input capacitance approximately equal to the input
10 capacitance of any one of the data signal comparators 110 and also to equal C_{R1} .
11 This ensures that integrated circuit 104 presents similar input impedances to both
12 the unbuffered reference voltage and the multiple signal voltages.

13 C_{R2} represents coupling capacitance of the *buffered* reference signal. This
14 capacitance is due primarily to the combined capacitances of the inputs of the
15 multiple signal comparators 110. Active buffer 112 is designed with a large
16 enough bandwidth to minimize the effects of C_{R2} and to thereby minimize any
17 noise injection through C_{R2} .

18 In the circuit of Fig. 5, noise induced by capacitive coupling in the
19 receiving integrated circuit will be largely common mode, since C_S equals C_{R1} and
20 since active buffer 112 has a sufficient bandwidth to largely negate any significant
21 noise injection through C_{R2} . In practice, active buffer 112 should have a
22 bandwidth that is significantly greater than the resonant input frequency of the
23 data signal line—a function of L_I and C_S . Specifically, the bandwidth of active
24 buffer 112 should be at least ten times greater than the resonant input frequency of
25 the data signal lines.

1 This circuit arrangement ensures that approximately equal coupled signal
2 noise is introduced in the distributed reference voltage and the plurality of pseudo-
3 differential signal voltages. Such common mode noise is canceled in the
4 comparisons performed by the signal comparators.

5 The described technique has been found to be extremely practical and
6 beneficial, especially in integrated circuits running at higher clock speeds and
7 having higher values of L_I .

8 Fig. 6 illustrates an alternative embodiment in which both the signal
9 voltages and the reference voltage are buffered. Specifically, the receiving
10 integrated circuit has a plurality of receivers or active buffers 202 that receive the
11 pseudo-differential signal voltages and in response produce buffered signal
12 voltages. Similarly, the reference voltage is routed to a single receiver or active
13 buffer 204 that produces a buffered reference voltage. The buffers need not have a
14 unity gain, but they do have approximately identical gains. In the described
15 embodiment, they are MOSFET-based source-followers.

16 Coupling capacitance associated with the signal voltage includes C_{S1} and
17 C_{S2} . C_{S1} represents coupling capacitance of the *unbuffered* signal voltage, and is a
18 result of capacitances of the input pad corresponding to the signal line, ESD
19 circuitry, and the input of the active buffer 202. Noise is injected into the
20 unbuffered signal line from the integrated circuit's substrate V_{SS} through coupling
21 capacitance C_{S1} .

22 C_{S2} represents coupling capacitance of the *buffered* signal voltage. This
23 capacitance is due primarily to the capacitance of the input of a signal comparator
24 210 associated with each signal line.
25

1 Coupling capacitance associated with the reference voltage includes C_{R1}
2 and C_{R2} . C_{R1} represents coupling capacitance of the *unbuffered*, undistributed
3 reference voltage, and is a result of capacitances of the input pad corresponding to
4 the reference line, ESD circuitry, and the input of the active buffer 204. Noise is
5 injected into the unbuffered reference line from the integrated circuit's substrate
6 V_{SS} through coupling capacitance C_{R1} .

7 C_{S2} represents coupling capacitance of the *buffered* and distributed
8 reference voltage. This capacitance is due primarily to the capacitance of the input
9 of signal comparator 210.

10 In this circuit, C_{S1} is approximately equal to C_{R1} . Thus, any noise injected
11 through these capacitances will be common mode. However, C_{R2} is significantly
12 greater than C_{S2} , due to the multitude of signal comparators whose inputs receive
13 the buffered reference voltage. Noise injected through these capacitances tends to
14 contain non-common mode components. However, such non-common mode
15 noise can be greatly reduced by designing the active buffer associated with the
16 reference line with much larger transistors than the active buffers associated with
17 the data signal lines. Specifically, active buffer 204 is designed to have an
18 electrical current capacity that is greater than the electrical current capacity of
19 active buffer 202 by a ratio equal to the ratio of C_{R2} to C_{S2} .

20 A larger buffer will usually have a higher input capacitance, which will
21 tend to make C_{R1} greater than C_{S1} . However, C_{R1} and C_{S1} are typically dominated
22 by ESD components so that the input capacitances of the active buffers have only
23 negligible effect. Furthermore, the signal line inputs can employ dummy
24 capacitors to equalize C_{R1} and C_{S1} .

Fig. 7 illustrates a third embodiment, appropriate for use in conjunction with two-stage input receivers. This embodiment comprises a plurality of two-stage input receivers 302, and a reference receiver or buffer 304. Input inductance and capacitance are represented in Fig. 7 as L_I and C_I , respectively. The circuit receives a plurality of signal voltages V_{SIGEXT} , which are subject to input inductance L_I and capacitance C_I to produce internal signal voltages referred to as V_{SIG} . The circuit also receives a voltage reference signal V_{REF} , which similarly subject to input inductance L_I and capacitance C_I to produce internal reference voltages referred to as V_{REFU} and V_{REFD} .

The first stage of a two-stage input receiver typically performs signal conditioning such as filtering, translating the input levels from the allowable input common-mode range to a fixed-output common-mode voltage, and converting the single-ended input into a differential output for the second stage. The second stage typically provides gain and performs latching.


In the circuit shown in Fig. 7, a two-stage input receiver 302 is provided for each incoming signal line. A first stage 310 of a receiver receives both a signal voltage V_{SIG} and a distributed reference voltage V_{REFD} . The term "distributed" in this context means that the reference voltage is provided to a plurality of receivers. First stage 310 conditions the signals and determines the voltage differential between them. This voltage differential is then provided to a second stage 312, in the form of a buffered differential voltage V_{BUF1} .

Reference receiver 304 has characteristics similar to first stages 310. Specifically, it has a similar or identical input impedance. In many cases, it is a duplicate of the circuits used within first stages 310.

1 Reference receiver 304 receives the distributed voltage V_{REFD} , and an
2 undistributed voltage V_{REFU} . V_{REFU} is a voltage or signal that has not been
3 distributed to all of the signal receivers. In this embodiment, the undistributed
4 reference voltage is connected to only to the single reference receiver 304.

5 The reference receiver is similar to the first stages 310 of the signal
6 receivers and performs similar functions. Specifically, it produces a buffered
7 differential voltage or signal V_{BUF2} , based on the voltage differential between its
8 two inputs—between V_{REFD} and V_{REFU} .

9 In operation, each V_{SIG} is subject to a load equal to the sum of the signal
10 line impedance (L_I and C_I) and the input impedance of first stage receiver 310.
11 V_{REFD} , however, is additionally subject to a load equal to sum of the signal line
12 impedance (L_I and C_I) and the cumulative input impedance of *all* the first stage
13 receivers 310. Because of this, noise is not produced equally in the distributed
14 reference voltage V_{REFD} as compared to each of the signal voltages V_{SIG} . In other
15 words, the difference between V_{SIG} and V_{REFD} will have a noise component equal
16 to the difference in noise between the signal voltage V_{SIG} and the distributed
17 reference voltage V_{REFD} . V_{REFU} , on the other hand, is subject to the load of only a
18 single receiver 304, just as the signal lines V_{SIG} .

19  The circuit of Fig. 6 works by generating a buffered voltage V_{BUF2} , which is
20 based at least in part on undistributed reference voltage V_{REFU} . Specifically, V_{BUF2}
21 is equal to V_{REFD} minus V_{REFU} : the difference between the relatively unloaded
22 reference voltage V_{REFU} as it is received and the more heavily loaded reference
23 voltage V_{REFD} after it is distributed to all of the input receivers 310. It also
24 represents the difference between the induced noise on V_{SIG} and the averaged
25 induced noise present on V_{REFD} .

1 To produce V_{BUF2} , both V_{REFD} and V_{REFU} are connected to the inputs of
2 reference receiver 304, which compares the two voltages and produces V_{BUF2} .
3 V_{BUF2} is distributed to the second stage 312 of each signal receiver 302. In
4 addition, the second stage receives the voltage produced by the first stage of the
5 signal receiver. To correct for noise, the second stage is configured to subtract
6 V_{BUF1} from V_{BUF2} . This results in a noise-compensated output voltage V_{OUT} .

7 Additional noise and signal degradation in V_{BUF2} are avoided by the use of
8 a differential output from reference receiver 304. First stage 310 also generates a
9 differential output, which avoids additional noise on V_{BUF2} . In addition, receivers
10 304 and 310 produce sampled outputs, so that the bandwidth of the amplifier
11 driving the noise signal is less critical—one can allocate some time for this
12 amplifier to settle.

13 A feature of this embodiment is that the noise (V_{BUF2}) is not distributed as a
14 full amplitude signal, equal to the reference voltage plus the noise. Rather, V_{BUF2}
15 in this embodiment represents only noise, and has much smaller amplitude than
16 the summed amplitude V_{BUF} of the previous embodiments.

17 The circuits described above improve the performance of pseudo-
18 differential signals, allowing smaller voltage differentials to be utilized so that
19 higher switching speeds can be attained.

20 Although the description above uses language that is specific to structural
21 features and/or methodological acts, it is to be understood that the invention
22 defined in the appended claims is not limited to the specific features or acts
23 described. Rather, the specific features and acts are disclosed as exemplary forms
24 of implementing the invention.
25